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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/663,774
Filing Date	September 17, 2003
First Named Inventor	Kyoung Mook LEE et al.
Art Unit	2871
Examiner Name	Dung T. Nguyen
Total Number of Pages in This Submission	
Attorney Docket Number	8733.915.00

ENCLOSURES (*Check all that apply*)

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension Request
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- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Signature	Eric J. Nuss
Date	June 4, 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kyoung Mook LEE et al.	Customer No. 30827
Application No. 10/663,774	Confirmation No. 1766
Filed: September 17, 2003	Art Unit: 2871
For: ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY AND FABRICATION METHOD THEREOF	Examiner: Dung T. Nguyen

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF

Sir:

In response to a Final Rejection of all pending claims that was mailed on November 3, 2006 and the Advisory Action of March 27, 2007, and in support of a "Notice of Appeal" filed April 3, 2007, Appellant hereby submits this Appeal Brief.

The fees required under § 37 C.F.R. §1.17(f) and any required petition for extension of time for filing this brief and fees therefore are provided for in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37(c):

I. Real Party In Interest

II. Related Appeals and Interferences

III. Status of Claims

IV. Status of Amendments

V. **Summary of Claimed Subject Matter**

VI. **Grounds of Rejection to be Reviewed on Appeal**

VII. **Argument**

VIII. **Claims Appendix**

IX. **Evidence Appendix**

X. **Related Proceedings Appendix**

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is: LG.PHILIPS LCD CO., LTD.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Total Number of Claims in the Application

There are 30 claims pending in the application.

Current Status of Claims:

Claims canceled: N/A.

Claims withdrawn from consideration but not canceled: N/A.

Claims pending: 1-30.

Claims allowed: None.

Claims rejected: 1-30.

Claims On Appeal: The claims on Appeal are claims 1-30.

IV. STATUS OF AMENDMENTS

The Examiner issued a Final Rejection on November 3, 2006 and an Advisory Action on March 27, 2007. No Amendment has been filed in response to this Final Rejection or Advisory Action. Accordingly, the claims enclosed in the Claims Appendix reflect the current status of claims 1-30.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following summary of the claimed subject matter includes a description of the independent claims 1, 8, 14 and 24. The present invention is directed to an array substrate for a liquid crystal display including a substrate (Figure 3, substrate 200); a plurality of gate lines (Figure 7, gate lines 411) and a plurality of thin film transistors (Figure 7, thin film transistors collectively elements 416, 420, 426 and 428) each having a gate electrode (Figure 7, gate electrode 420), a source electrode (Figure 7, source electrode 426) a drain electrode (Figure 7, drain electrode 428) and an active layer (Figure 7, active layer 416) formed over the substrate (Figure 3, substrate 200); an interlayer insulating layer formed on the thin film transistors (Figure 3, interlayer insulating layer 224); a first gate redundancy line (Figure 3, gate redundancy line 229) formed on the interlayer insulating layer (Figure 3, interlayer insulating layer 224), and connected electrically with just one of the gate electrodes (420), one of the gate lines (Figure 7, gate lines 411), and both gate electrode (420) and gate line (411) through a first gate contact hole (Figure 3, gate contact hole 239) and formed of the same material as one of the source and drain electrodes (Specification [0066] page 11); a passivation layer provided on the first gate redundancy line and the interlayer insulating layer (Figure 3, passivation layer 232); and a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer (Figure 3, pixel electrode 234, drain electrode 228 and drain contact hole 230).

An array substrate for a liquid crystal display includes: a substrate (Figure 3, substrate 200); a plurality of gate lines (Figure 7, gate lines 411) and a plurality of thin film transistors (Figure 7, thin film transistors collectively elements 416, 420, 426 and 428) each having a gate electrode (Figure 7, gate electrode 420), a source electrode (Figure 7, source electrode 426), a drain electrode (Figure 7, drain electrode 428) and an active layer (Figure 7, active layer 416) formed on the substrate (Figure 3, substrate 200); an interlayer insulating layer formed on the thin film transistors (Figure 3, interlayer insulating layer 224); a passivation layer formed on the interlayer insulating layer (Figure 3, passivation layer 232); a pixel electrode (Figure 3, pixel electrode 234) electrically connected with the drain electrode (Figure 3, drain electrode 228) through a drain contact hole formed in the passivation layer (Figure 3, drain contact hole 230); and a gate redundancy line formed on the passivation layer (Figure 3, gate redundancy line 229),

and connected electrically with just one of the gate electrodes (420), the gate lines (411), and both gate electrode (420) and gate line (411) through a gate contact hole (Figure 3, gate contact hole (239) and formed of the same material as the pixel electrode (Specification referring to Figure 5, [0098] page 15).

A method of fabricating an array substrate for a liquid crystal display includes in reference to Figures 4A-4D: forming a plurality of gate lines (gate lines 411 from Figure 7) and gate electrodes (220) on a substrate (200); forming an interlayer insulating layer (224) on the gate lines (Figure 7, 411) and the gate electrodes (420); forming a plurality of thin film transistors with the gate electrodes (220), source electrodes (226), drain electrodes (228), and active layers (216); forming a first gate redundancy line (229) on the interlayer insulating layer (224) electrically connected with just one of the gate electrodes (420), the gate lines (Figure 7, 411), and both the gate electrode (420) and gate line (411) through a first gate contact hole (239); forming a passivation layer (232) on the first gate redundancy line (229) and the interlayer insulating layer (224); and forming a drain contact hole (230) in the passivation layer (232), and forming a pixel electrode (234) connected electrically with the drain electrode (228) through the drain contact hole (230).

A method of fabricating an array substrate for a liquid crystal display includes in reference to Figures 6A-6D: forming a plurality of gate lines (Figure 7, gate lines 411) and gate electrodes (320) on a substrate (300); forming an interlayer insulating layer (324) on the gate line (Figure 7, gate line 411) and the gate electrode (320); forming a plurality of thin film transistors with gate electrodes (320), source electrodes (326), drain electrodes (328), and active layers (316); forming a passivation layer (332) on the interlayer insulating layer (324) and the thin film transistors; and forming a gate contact hole (339) in the passivation layer (332), and forming a gate redundancy line (329) connected electrically with just one of the gate electrodes (320), the gate lines (Figure 7, 411), and both gate electrode (320) and gate line (Figure 7, gate line 411) through the gate contact hole (339).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner rejected claims 1-30 under 35 U.S.C. §103(a) as unpatentable over WO 03/058332 A1 (to Lee et al.)(hereinafter "Lee").

VII. ARGUMENT

A. The Examiner improperly rejected claims 1-7 under 35 U.S.C. § 103(a) as allegedly unpatentable over Lee.

Claims 1-7

In rejecting claim 1, the Examiner equates Lee's reference number 170 with that of Appellant's first gate redundancy line. The Examiner equates Lee's reference number 175 with that of Appellant's second gate redundancy line. However, Lee's reference number 170 refers to *a gate pad electrode* and 175 refers to a *pad contact hole*. Clearly, the Lee elements identified by the Examiner are not those as claimed by Appellant.

In the Advisory Action of March 27, 2007, the Examiner states, "it is note that the gate pad electrode can be a redundancy line as well (see page 16) and inherently connected to the gate line." It is not at all clear as to what "page 16" the Examiner refers. Furthermore, as best understood, a gad pad electrode exists on the periphery of a device. Appellant's gate redundancy lines are formed *internal* to the device and *not on the periphery* of the device as can be seen in Appellant's Figures.

In addition, the Examiner did not address at least the claimed limitation, "a first gate redundancy line formed on the interlayer insulating layer, and connected electrically with just one of the gate electrodes, one of the gate lines, and both gate electrode and gate line through a first gate contact hole." This limitation was not addressed in the Final Rejection of November 3, 2006 and not addressed at all in the Advisory Action of March 27, 2007.

Furthermore, the Examiner states that, "Lee et al., however, do not disclose the first gate redundancy line being formed of the same material as one of the source and drain electrode. It would have been obvious to one skilled in the art at the time of the invention was mad to form a gate redundancy electrode and source/drain electrode having a same based material, since it is a common practice in the art to simplify process steps for forming an LCD device." (Office Action at page 3). The Examiner's taking what appears to be Official Notice is seasonably traversed and objected to by Appellant. There may be other reasons for forming a gate redundancy line of the same material as source and drain electrodes other than those reasons provided by the Examiner.

For example, choice of materials for redundancy lines and source and drain electrodes may be a function of line resistance and signal delay.

Furthermore, Appellant respectfully notes that the Examiner did not address the limitation, "a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer." This limitation was not addressed in the Final Rejection of November 3, 2006 and not addressed at all in the Advisory Action of March 27, 2007. Claims 2-7 depend either directly or indirectly from claim 1 and implicitly include all of the limitations of claim 1. Accordingly, Appellant respectfully submits that the Examiner has not made a *prima facie* case of obviousness of claims 2-7 at least because of the respective dependencies of claims 2-7 and because of the reasons given for claim 1.

B. The Examiner improperly rejected claims 8-13 under 35 U.S.C. § 103(a) as allegedly unpatentable over Lee.

Claims 8-13

In rejecting claim 8, The Examiner did not address at all " ... a pixel electrode electrically connected with the drain electrode through a drain contact hole formed in the passivation layer; and a gate redundancy line formed on the passivation layer, and connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through a gate contact hole and formed of the same material as the pixel electrode."

Further, Appellant's arguments with respect to the rejection of claims 1-7 apply equally to the rejection of claims 8-13. Accordingly, Appellant respectfully submits that the Examiner has not made a *prima facie* case of obviousness of claims 9-13 at least because of the respective dependencies of claims 9-13 and because of the reasons given for claim 8.

C. The Examiner improperly rejected claims 14-23 under 35 U.S.C. § 103(a) as allegedly unpatentable over Lee.

Claims 14-23

In rejecting claim 14, drawn to a method of fabricating an array substrate for a liquid crystal display, the Examiner did not address any method limitations. In the Advisory Action of

March 27, 2007, the Examiner states, "the *device claims* do not define over the art of record (as stated in the final office action)(emphasis added)." There is no mention of the method claims in the Advisory Action. Further, Appellant's arguments with respect to the rejection of claims 1-13 apply equally to the rejection of claims 14-23.

Claims 15-23 depend either directly or indirectly from claim 14 and implicitly include all of the limitations of claim 14. Accordingly, Appellant respectfully submits that the Examiner has not made a *prima facie* case of obviousness of claims 15-23 at least because of the respective dependencies of claims 15-23 and because of the reasons given for claim 14.

D. The Examiner improperly rejected claims 24-30 under 35 U.S.C. § 103(a) as allegedly unpatentable over Lee.

Claims 24-30

In rejecting claim 24, drawn to a method of fabricating an array substrate for a liquid crystal display, the Examiner did not address any method limitations. In the Advisory Action of March 27, 2007, the Examiner states, "the *device claims* do not define over the art of record (as stated in the final office action)(emphasis added)." There is no mention of the method claims in the Advisory Action. Further, Appellant's arguments with respect to the rejection of claims 1-23 apply equally to the rejection of claims 24-30.

Appellant furthermore seasonably traverses and objects to the Examiner's taking Official Notice with respect to the rejection of claims 2, 9, 16 and 26 (Office Action at page 3). In rejecting claims 2, 9, 16 and 26, the Examiner states, "although Lee et al. do not explicitly disclose a top gate type TFT, it would have been an obvious to one having ordinary skill in the art at the time the invention was made to employ the Lee et al device having a top gate TFT since the examiner takes Office Notice of the equivalence of a top gate type TFT and a bottom type TFT for their use in the display art and the selection of any of these known equivalents to operate a display device would be within the level of ordinary skill in the art." (Office Action at page 3).

Appellant respectfully notes that top gate and bottom gate TFTs are manufactured by very different processes. At least claims 16, 18, 26 and 28 are method claims claiming the fabrication method of an array substrate in either top or bottom gate TFT *manner*. That is, these

claims are not just device limitations but require a *manner* of formation. Accordingly, the Examiner's taking of Official Notice is inappropriate.

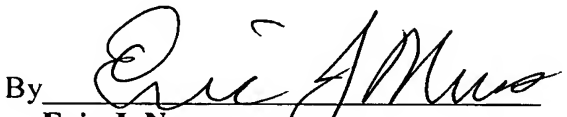
Claims 25-30 depend either directly or indirectly from claim 24 and implicitly include all of the limitations of claim 24. Accordingly, Appellant respectfully submits that the Examiner has not made a *prima facie* case of obviousness of claims 25-30 at least because of the respective dependencies of claims 25-30 and because of the reasons given for claim 24.

A copy of the claims involved in the present Appeal is attached hereto as the Claims Appendix.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: June 4, 2007

By 

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CLAIMS APPENDIX

Claims Involved In The Appeal Of Application No. 10/663,774:

1. (Previously Presented) An array substrate for a liquid crystal display, the array substrate comprising:

a substrate;

a plurality of gate lines and a plurality of thin film transistors each having a gate electrode, a source electrode, a drain electrode and an active layer formed over the substrate;

an interlayer insulating layer formed on the thin film transistors;

a first gate redundancy line formed on the interlayer insulating layer, and connected electrically with just one of the gate electrodes, one of the gate lines, and both gate electrode and gate line through a first gate contact hole and formed of the same material as one of the source and drain electrodes;

a passivation layer provided on the first gate redundancy line and the interlayer insulating layer; and

a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer.

2. (Original) The array substrate according to claim 1, wherein the thin film transistor is a top-gate thin film transistor.

3. (Original) The array substrate according to claim 2, wherein the first gate contact hole is formed passing through the interlayer insulating layer.

4. (Original) The array substrate according to claim 1, wherein the thin film transistor is a bottom-gate thin film transistor.

5. (Original) The array substrate according to claim 4, wherein the first gate contact hole is formed passing through the gate insulating layer and the interlayer insulating layer.

6. (Original) The array substrate according to claim 1, further comprising a second gate redundancy line formed on the passivation layer, and connected electrically with the first

gate redundancy line through a second gate contact hole and formed of the same material as the pixel electrode.

7. (Previously Presented) The array substrate according to claim 1, wherein the first gate redundancy line electrically connects with a gate line though a second gate contact hole.

8. (Previously Presented) An array substrate for a liquid crystal display, the array substrate comprising:

a substrate;

a plurality of gate lines and a plurality of thin film transistors each having a gate electrode, a source electrode, a drain electrode and an active layer formed on the substrate;

an interlayer insulating layer formed on the thin film transistors;

a passivation layer formed on the interlayer insulating layer;

a pixel electrode electrically connected with the drain electrode through a drain contact hole formed in the passivation layer; and

a gate redundancy line formed on the passivation layer, and connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through a gate contact hole and formed of the same material as the pixel electrode.

9. (Original) The array substrate according to claim 8, wherein the thin film transistor is a top-gate thin film transistor.

10. (Original) The array substrate according to claim 9, wherein the gate contact hole is formed passing through the interlayer insulating layer and passivation layer.

11. (Original) The array substrate according to claim 8, wherein the thin film transistor is a bottom-gate thin film transistor.

12. (Original) The array substrate according to claim 11, wherein the gate contact hole is formed passing through the gate insulating layer, the interlayer insulating layer, and the passivation layer.

13. (Previously Presented) The array substrate according to claim 8, wherein the gate redundancy line electrically connects with a gate line though a second gate contact hole.

14. (Previously Presented) A method of fabricating an array substrate for a liquid crystal display, the method comprising:

forming a plurality of gate lines and gate electrodes on a substrate;

forming an interlayer insulating layer on the gate lines and the gate electrodes;

forming a plurality of thin film transistors with the gate electrodes, source electrodes, drain electrodes, and active layers;

forming a first gate redundancy line on the interlayer insulating layer electrically connected with just one of the gate electrodes, the gate lines, and both the gate electrode and gate line through a first gate contact hole;

forming a passivation layer on the first gate redundancy line and the interlayer insulating layer; and

forming a drain contact hole in the passivation layer, and forming a pixel electrode connected electrically with the drain electrode through the drain contact hole.

15. (Original) The fabrication method according to claim 14, wherein the first gate redundancy line is formed with the same process and of the same material as one of the source electrode and drain electrode.

16. (Original) The fabrication method according to claim 14, wherein the thin film transistor having the gate electrode and the source electrode, and the drain electrode is formed in a top-gate manner.

17. (Original) The fabrication method according to claim 16, wherein the first gate contact hole is formed passing through the interlayer insulating layer.

18. (Original) The fabrication method according to claim 14, wherein thin film transistor having the gate electrode and the source electrode, and the drain electrode is formed in a bottom-gate manner.

19. (Original) The fabrication method according to claim 18, including forming a gate insulating layer between the gate electrode and the active layer, wherein the first gate contact hole is formed passing through the gate insulating layer and the interlayer insulating layer.

20. (Original) The fabrication method according to claim 14, further comprising forming a second gate redundancy line on the passivation layer connected electrically with the first gate redundancy line through a second gate contact hole.

21. (Original) The fabrication method according to claim 20, wherein the second gate redundancy line is formed in the same process and of the same material as the pixel electrode.

22. (Original) The fabrication method according to claim 20, wherein the second gate contact hole is formed passing through the passivation layer on the first gate redundancy line.

23. (Original) The fabrication method according to claim 14, further comprising forming a second gate contact hole wherein the first gate redundancy line electrically connects with the gate line though the second gate contact hole.

24. (Previously Presented) A method of fabricating an array substrate for a liquid crystal display, the method comprising:

forming a plurality of gate lines and gate electrodes on a substrate;

forming an interlayer insulating layer on the gate line and the gate electrode;

forming a plurality of thin film transistors with gate electrodes, source electrodes, drain electrodes, and active layers;

forming a passivation layer on the interlayer insulating layer and the thin film transistors; and

forming a gate contact hole in the passivation layer, and forming a gate redundancy line connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through the gate contact hole.

25. (Original) The fabrication method according to claim 24, wherein the gate redundancy line is formed with the same process and the same material as the pixel electrode.

26. (Original) The fabrication method according to claim 24, wherein the thin film transistor is formed in a top-gate manner.

27. (Original) The fabrication method according to claim 26, wherein the gate contact hole is formed passing through the interlayer insulating layer and passivation layer.

28. (Original) The fabrication method according to claim 24, wherein the thin film transistor is formed in a bottom-gate manner.

29. (Original) The fabrication method according to claim 28, including forming a gate insulating layer between the gate electrode and the active layer, wherein the gate contact hole is formed passing through the gate insulating layer, the interlayer insulating layer, gate insulating layer and the passivation layer.

30. (Original) The fabrication method according to claim 24, further comprising forming a second gate contact hole in the passivation layer and interlayer insulating layer wherein the gate redundancy line electrically connects with the gate line though a second gate contact hole.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

Related Proceedings:

None.